

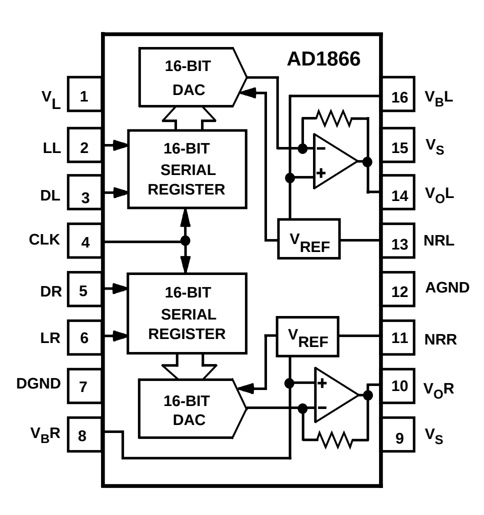
Single Supply Dual 16-Bit Audio DAC

AD1866*

FEATURES
Dual Serial Input, Voltage Output DACs
Single +5 Volt Supply
0.005% THD+N
Low Power –50 mW
115 dB Channel Separation
Operates at 8× Oversampling
16-Pin Plastic DIP or SOIC Package

APPLICATIONS
Multimedia Workstations
PC Audio Add-In Boards
Portable CD and DAT Players
Automotive CD and DAT Players
Noise Cancellation

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1866 is a complete dual 16-bit DAC offering excellent performance while requiring a single +5 V power supply. It is fabricated on Analog Devices' ABCMOS wafer fabrication process. The monolithic chip includes CMOS logic elements, bipolar and MOS linear elements and laser trimmed, thin-film resistor elements. Careful design and layout techniques have resulted in low distortion, low noise, high channel separation and low power dissipation.

The DACs on the AD1866 chip employ a partially segmented architecture. The first three MSBs of each DAC are segmented into 7 elements. The 13 LSBs are produced using standard R-2R techniques. The segments and R-2R resistors are laser trimmed to provide extremely low total harmonic distortion. The AD1866 requires no deglitcher or trimming circuitry.

Each DAC is equipped with a high performance output amplifier. These amplifiers achieve fast settling and high slew rate, producing ±1 V signals at load currents up to ±1 mA. The buffered output signal range is 1.5 V to 3.5 V. The 2.5 V reference voltages eliminate the need for "false ground" networks.

A versatile digital interface allows the AD1866 to be directly connected to all digital filter chips. Fast CMOS logic elements allow for an input clock rate of up to 16 MHz. This allows for operation at 2×, 4×, 8×, or 16× the sampling frequency (where F_S = 44.1 kHz) for each channel. The digital input pins of the AD1866 are TTL and +5 V CMOS compatible.

The AD1866 operates on +5 V power supplies. The digital supply, V_L, can be separated from the analog supply, V_S, for reduced digital feedthrough. Separate analog and digital ground pins are also provided. In systems employing a single +5 volt power supply, V_L and V_S should be connected together. In battery operated systems, operation will continue even with reduced supply voltage. Typically, the AD1866 dissipates 50 mW.

The AD1866 is packaged in either a 16-pin plastic DIP or a 16-pin plastic SOIC package. Operation is guaranteed over the temperature range of –35°C to +85°C and over the voltage supply range of 4.75 V to 5.25 V.

PRODUCT HIGHLIGHTS

1. Single supply operation @ +5 V.
2. 50 mW power dissipation.
3. THD+N is 0.005% (typical).
4. Signal-to-Noise Ratio is 95 dB (typical).
5. 115 dB channel separation (typical).
6. Compatible with all digital filter chips.
7. 16-pin DIP and 16-pin SOIC packages.
8. No deglitcher required.
9. No external adjustments required.

***Protected by U.S. Patent Nos: 3,961,326; 4,141,004; 4,349,811; 4,857,862; and patents pending.**

REV. 0

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AD1866—SPECIFICATIONS (T_A = +25°C and +5 V supplies unless otherwise noted)

		Min	Typ	Max	Unit
RESOLUTION			16		Bits
DIGITAL INPUTS	V_{IH}	**2.4**			V
	V_{IL}			**0.8**	V
	I_{IH}, $V_{IH} = V_L$		1.0		µA
	I_{IL}, V_{IL} = DGND		–10.0		µA
Maximum Clock Input Frequency		**13.5**			MHz
ACCURACY					
Gain Error			±3		% of FSR
Gain Matching			±3		% of FSR
Midscale Error			±30		mV
Midscale Error Matching			±10		mV
Gain Linearity Error			±3		dB
DRIFT (0°C to +70°C)					
Gain Drift			±100		ppm/°C
Midscale Drift			–130		µV/°C
TOTAL HARMONIC DISTORTION + NOISE					
0 dB, 990.5 Hz	AD1866N		0.005	**0.01**	%
	AD1866R		0.005	**0.01**	%
–20 dB, 990.5 Hz	AD1866N		0.02		%
	AD1866R		0.02		%
–60 dB, 990.5 Hz	AD1866N		2.0		%
	AD1866R		2.0		%
CHANNEL SEPARATION (1 kHz, 0 dB)		**108**	115		dB
SIGNAL-TO-NOISE RATIO (With A-Weight Filter)			95		dB
D-RANGE (With A-Weight Filter)			90		dB
OUTPUT					
Voltage Output Pins (V_{OL}, V_{OR})					
Output Range (±3%)			±1		V
Output Impedance			0.1		Ω
Load Current			±1		mA
Bias Voltage Pins (V_{BL}, V_{BR})					
Output Range			+2.5		V
Output Impedance			350		Ω
POWER SUPPLY					
Specification, V_L and V_S		**4.75**	5	**5.25**	V
Operation, V_L and V_S		**3.5**		**5.25**	V
+I, V_L and V_S = 5 V			10	**14**	mA
POWER DISSIPATION			50	70	mW
TEMPERATURE RANGE					
Operation		–35		**85**	°C
Storage		–60		**100**	°C

Specifications subject to change without notice.
Specifications in **boldface** are tested on all production units at final electrical

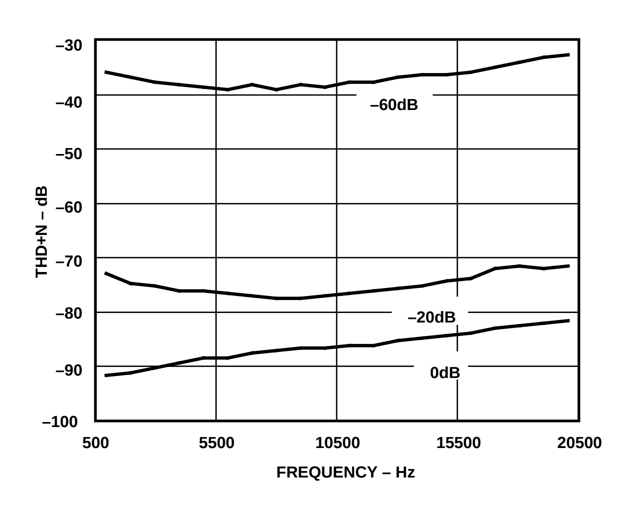


Figure 1. THD+N vs. Frequency

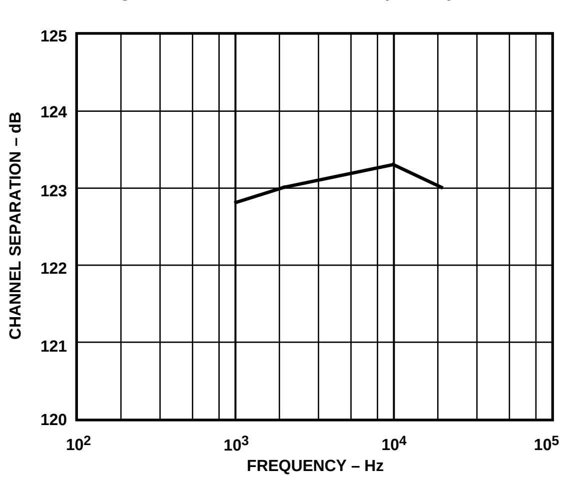


Figure 2. Channel Separation vs. Frequency

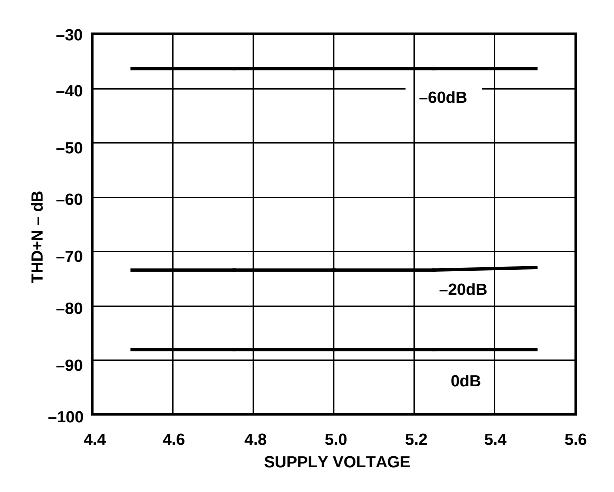


Figure 3. THD+N vs. Supply Voltage

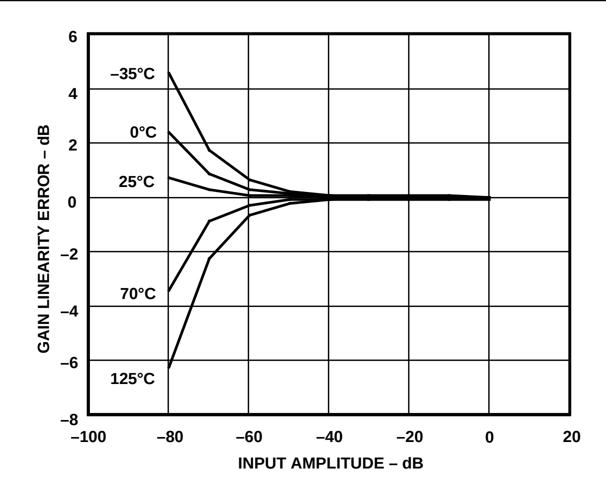


Figure 4. Gain Linearity Error vs. Input Amplitude

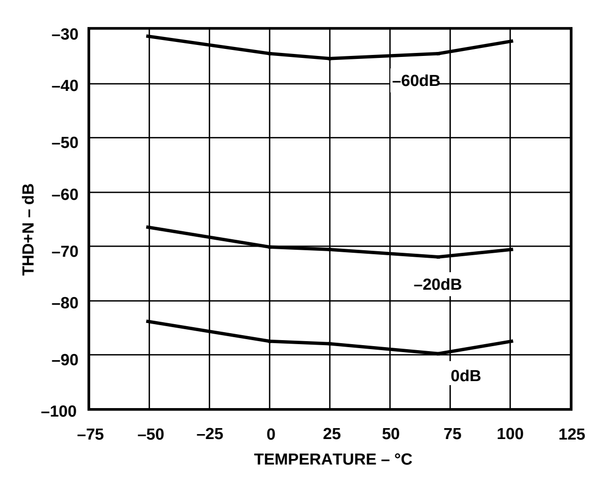


Figure 5. THD+N vs. Temperature

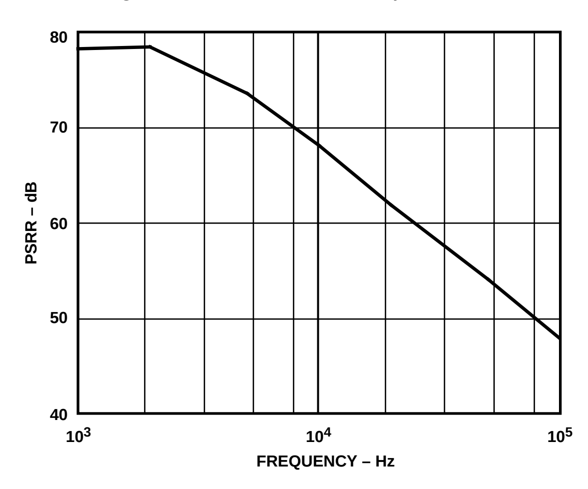


Figure 6. Power Supply Rejection Ratio vs. Frequency (Supply Modulation Amplitude at 500 mV p-p)

ABSOLUTE MAXIMUM RATINGS*

V_L to DGND . . . . 0 V to 6 V
V_S to AGND . . . . 0 V to 6 V
AGND to DGND . . . . ±0.3 V
Digital Inputs to DGND . . . . –0.3 V to V_L
Soldering (10 sec) . . . . +300°C

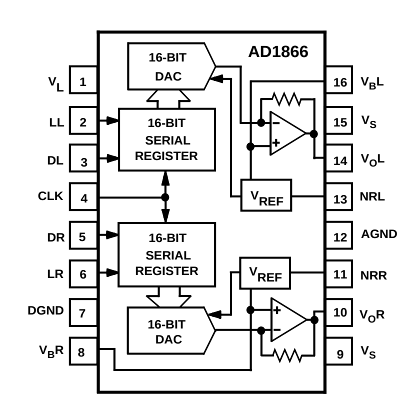
*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1866 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION



PIN DESIGNATIONS

Pin	Mnemonic	Description
1	V_L	Digital Supply (+5 V)
2	LL	Left Channel Latch Enable Pin
3	DL	Left Channel Data Input Pin
4	CLK	Clock Input Pin
5	DR	Right Channel Data Input Pin
6	LR	Right Channel Latch Enable Pin
7	DGND	Digital Common Pin
8	V_BR	Right Channel Bias Pin
9	V_S	Analog Supply (+5 V)
10	V_OR	Right Channel Output Pin
11	NRR	Right Channel Noise Reduction Pin
12	AGND	Analog Common Pin
13	NRL	Left Channel Noise Reduction Pin
14	V_OL	Left Channel Output Pin
15	V_S	Analog Supply (+5 V)
16	V_BL	Left Channel Bias Pin

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD1866N	–35°C to +85°C	Plastic DIP	N-16
AD1866R	–35°C to +85°C	SOIC	R-16
AD1866R-REEL	–35°C to +85°C	SOIC	R-16

TOTAL HARMONIC DISTORTION + NOISE

Total harmonic distortion plus noise (THD+N) is defined as the ratio of the square root of the sum of the squares of the amplitudes of the harmonics and noise to the amplitude of the fundamental input frequency. It is usually expressed in percent (%) or decibels (dB).

D-RANGE DISTORTION (EIAJ SPECIFICATION)

D-Range distortion is the ratio of the amplitude of the signal at an amplitude of –60 dB to the amplitude of the distortion plus noise. In this case, an A-weight filter is used. The value specified for D-range performance is the ratio measured plus 60 dB.

SIGNAL-TO-NOISE RATIO

The signal-to-noise ratio is defined as the ratio of the amplitude of the output when a full-scale output is present to the amplitude of the output with no signal present. It is expressed in decibels (dB) and measured using an A-weight filter.

GAIN LINEARITY

Gain linearity is a measure of the deviation of the actual output amplitude from the ideal output amplitude. It is determined by measuring the amplitude of the output signal as the amplitude of that output signal is digitally reduced to a lower level. A perfect D/A converter exhibits no difference between the ideal and actual amplitudes. Gain linearity is expressed in decibels (dB).

MIDSCALE ERROR

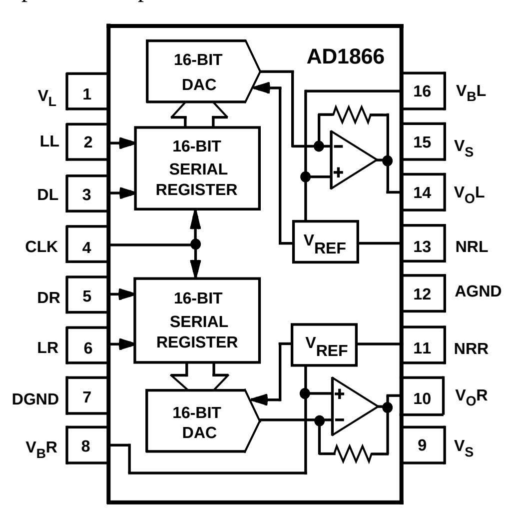
Midscale error, or bipolar zero error, is the deviation of the actual analog output from a voltage at the bias pin when the twos complement input code representing midscale is loaded in the DAC. Midscale error is expressed in mV.

FUNCTIONAL DESCRIPTION

The AD1866 is a complete, monolithic dual 16-bit digital audio DAC which runs off a single +5 volt supply. As shown in the block diagram, each channel contains a voltage reference, a 16-bit serial-to-parallel input register, a 16-bit input latch, a 16-bit DAC, and an output amplifier.

The voltage reference section provides a reference voltage and a false ground voltage for each channel. The low noise bandgap circuits produce reference voltages that are unaffected by changes in temperature, time, and power supply.

The input registers are fabricated with CMOS logic gates. These gates allow high switching speeds and low power consumption, contributing to the fast digital timing, the low glitch and low power dissipation of the AD1866.



AD1866 Functional Block Diagram

The 16-bit DAC uses a combination of segmentation and R-2R architecture to achieve good integral and differential linearity. The resistors which form the ladder structure are fabricated with silicon-chromium thin film. Laser trimming of these resistors further reduces linearity error, resulting in low output distortion.

The output amplifier uses both MOS and bipolar devices and incorporates an NPN class A output stage. It is designed to produce high slew rate, low noise, low distortion, and optimal frequency response.

AD1866–Analog Circuit Considerations

GROUNDING RECOMMENDATIONS

The AD1866 has two ground pins, designated as AGND (Pin 12) and DGND (Pin 7). The analog ground, AGND, serves as the "high quality" reference ground for analog signals and as a return path for the supply current from the analog portion of the device. The system analog common should be located as close as possible to Pin 12 to minimize any voltage drop which may develop between these two points, although the internal circuit is designed to minimize signal dependence of the analog return current.

The digital ground, DGND, returns ground current from the digital logic portion of the device. This pin should be connected to the digital common node in the system. As shown in Figure 7, the analog and digital grounds should be joined at one point in a system. When these two grounds are connected such as at the power supply ground, care should be taken to minimize the voltage difference between the DGND and AGND pins in order to ensure the specified performance.

POWER SUPPLIES AND DECOUPLING

The AD1866 has three power supply input pins. V_S (Pins 9 and 15) provide the supply voltages which operate the analog portion of the device including the 16-bit DACs, the voltage references, and the output amplifiers. The V_S supplies are designed to operate from a +5 V supply. These pins should be decoupled to the analog ground using a 0.1 µF capacitor. Good engineering practice suggests that the bypass capacitor be placed as close as possible to the package pins. This minimizes the inherent inductive effects of printed circuit board traces.

V_L (Pin 1) operates the digital portions of the chip including the input shift registers and the input latching circuitry. V_L is also designed to operate from a +5 V supply. This pin should be bypassed to digital common using a 0.1 µF capacitor, again placed as close as possible to the package pins. Figure 7 illustrates the correct connection of the digital and analog supply bypass capacitors.

An important feature of the AD1866 audio DAC is its ability to operate at diminished power supply voltages. This feature is very important in portable battery operated systems. As the batteries discharge, the supply voltage drops. Unlike any other audio DAC, the AD1866 can continue to function at supply voltages as low as 3.5 V. Because of its unique design, the power requirements of the AD1866 diminish as the battery voltage drops, further extending the operating time of the system.

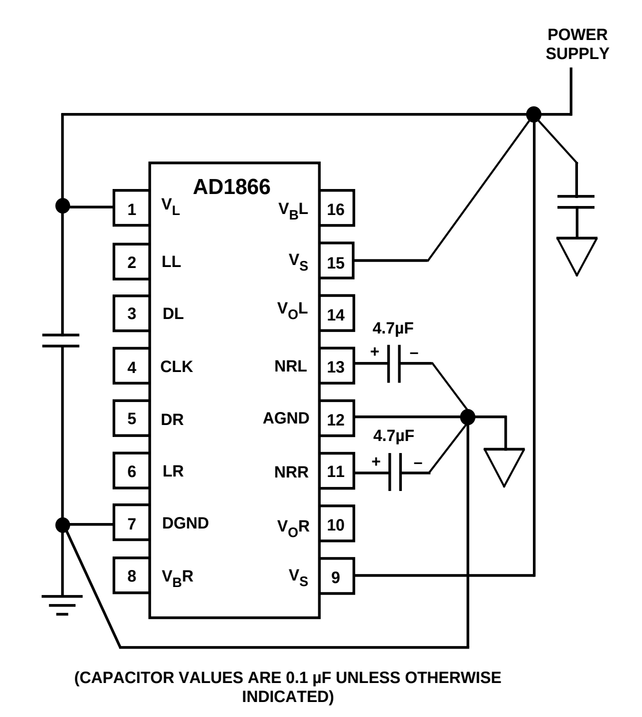


Figure 7. Recommended Circuit Schematic

NOISE REDUCTION CAPACITORS

The AD1866 has two noise reduction pins, designated as NRL (Pin 13) and NRR (Pin 11). In order to meet specifications, it is required that external noise reduction capacitors be connected from these pins to AGND to reduce the output noise contributed by the voltage reference circuitry. As shown in Figure 7, each of these pins should be bypassed to AGND with a 4.7 µF or larger capacitor. The connections between the capacitors, package pins and AGND should be as short as possible to achieve the lowest noise.

USING V_BL AND V_BR

The AD1866 has two bias voltage reference pins, designated as V_BR (Pin 8) and V_BL (Pin 16). Each of these pins supplies a dc reference voltage equal to the center of the output voltage swing. These bias voltages replace "false ground" networks previously required in single supply audio systems. At the same time, they allow dc coupled systems, improving audio performance.

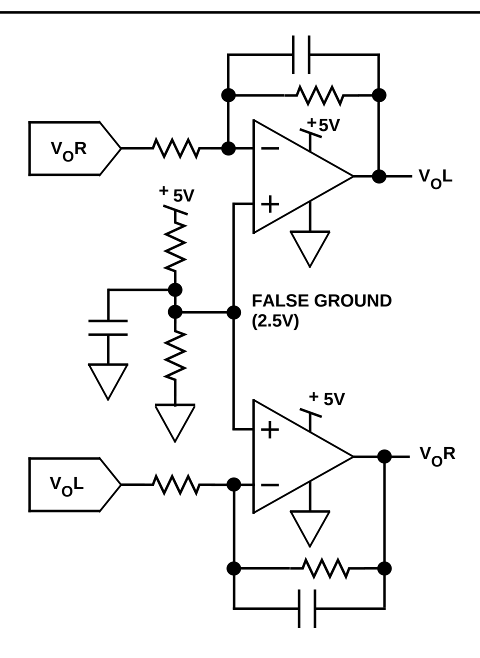


Figure 8a. Schematic Using False Ground

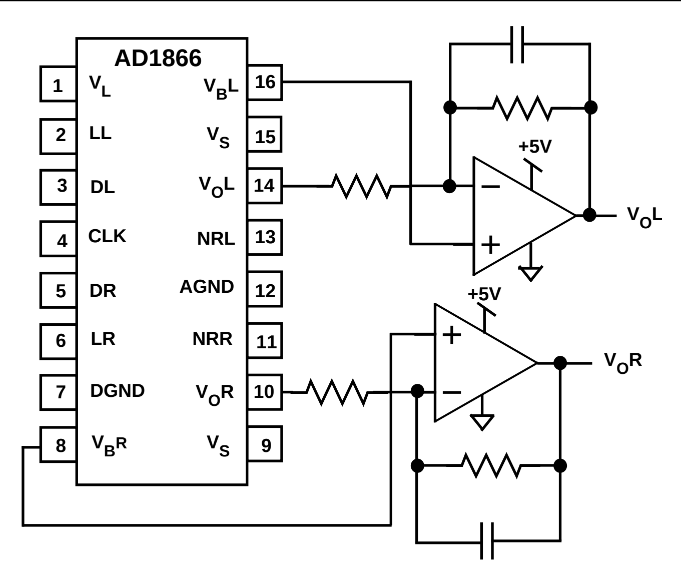


Figure 8b. Circuitry Using Voltage Biases

Figure 8a illustrates the traditional approach used to generate false ground voltages in single supply audio systems. This circuit requires additional power and circuit board space.

The AD1866 eliminates the need for "false ground" circuitry. V_BR and V_BL generate the required bias voltages previously generated by the "false ground." As shown in Figure 8b, V_BR and V_BL may be used as the reference point in each output channel. This permits a dc coupled output signal path. This eliminates ac coupling capacitors and improves low frequency performance. It should be noted that these bias outputs have relatively high output impedance and will not drive output currents larger than 100 µA without degrading the specified performance.

DISTORTION PERFORMANCE AND TESTING

The THD+N figure of an audio DAC represents the amount of undesirable signal produced during reconstruction and playback of an audio waveform. Therefore, the THD+N specification provides a direct measure to classify and choose an audio DAC for a desired level of performance. Figure 1 illustrates the typical THD+N versus frequency performance of the AD1866. It is evident that the THD+N performance of the AD1866 remains stable at all three amplitude levels through a wide range of frequencies. A load impedance of at least 2 kΩ is recommended for best THD+N performance.

Analog Devices tests all AD1866s on the basis of THD+N performance. During the distortion test, a high speed digital pattern generator transmits digital data to each channel of the device under test. Sixteen-bit data is latched into the DAC at 352.8 kHz (8 × F_S). The test input code is a digitally encoded 990.5 Hz sine wave with 0 dB, –20 dB, and –60 dB amplitudes. A 4096 point FFT calculates total harmonic distortion + noise, signal-to-noise ratio, and D-range. No deglitchers or external adjustments are used.

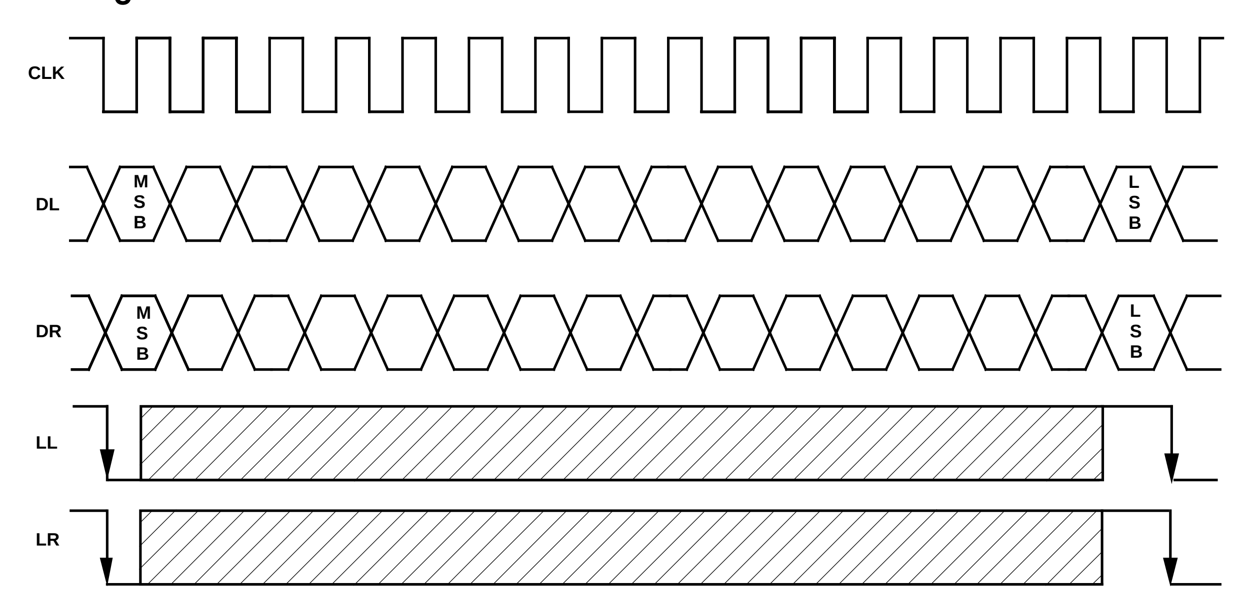


Figure 9. AD1866 Control Signals

INPUT DATA

The digital input port of the AD1866 employs five signals: Data Left (DL), Data Right (DR), Latch Left (LL), Latch Right (LR), and Clock (CLK). DL and DR are the serial inputs for the left and right DACs, respectively. Input data bits are clocked into the input register on the rising edge of CLK. The falling edges of LL and LR cause the last 16 bits which were clocked into the serial registers to be shifted into the DACs, thereby updating the respective DAC outputs. For systems using only a single latch signal, LL and LR may be connected together. For systems using only one DATA signal, DR and DL may be connected together. Data is transmitted to the AD1866 in a bit stream composed of 16-bit words with a serial, twos complement, MSB first format. Left and right channels share the Clock (CLK) signal.

Figure 9 illustrates the general signal requirements for data transfer for the AD1866.

TIMING

Figure 10 illustrates the specific timing requirements that must be met in order for the data transfer to be accomplished properly. The input pins of the AD1866 are both TTL and +5 V CMOS compatible.

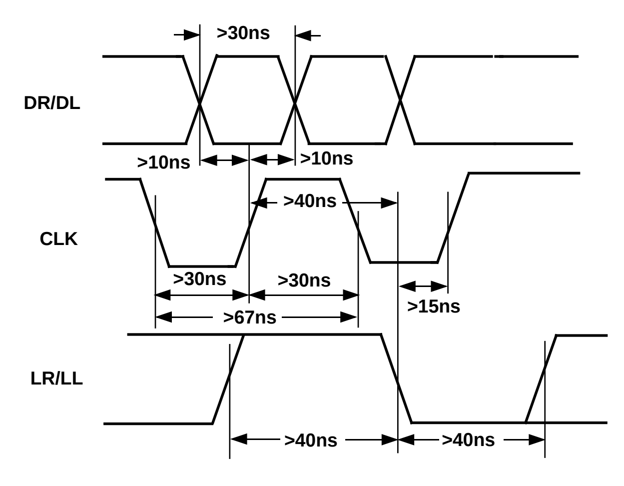


Figure 10. AD1866 Input Signal Timing

The maximum clock rate of the AD1866 is specified to be at least 13.5 MHz. This clock rate allows data transfer rates of 2×, 4×, 8×, and 16× F_S (where F_S equals 44.1 kHz). The applications section of this data sheet contains additional guidelines for using the AD1866.

APPLICATIONS OF THE AD1866

The AD1866 is a high performance audio DAC specifically designed for portable and automotive digital audio applications. These market segments have technical requirements fundamentally different than those found in the high-end or home use market segment. Portable equipment must rely on components which require low amounts of power to offer reasonable playback times. Also, battery voltage tends to diminish as the end of the discharge cycle is approached. The AD1866's ability to operate from a single +5 V supply makes it a good choice for battery operated gear. And, as the battery voltage drops, the power dissipation of the AD1866 drops. This extends the usable battery life. Finally, as the battery supply voltage drops, the bias voltages and signal swings also drop, preventing signal clipping and abrupt degradation of distortion. Figure 3 illustrates how the THD+N performance of the AD1866 remains constant through a wide supply voltage range.

Automotive equipment relies on components which are able to consistently perform over a wide range of temperatures. In addition, due to the limited space available in automotive applications, small size is essential. The AD1866 has guaranteed operation between –35°C and +85°C, and the 16-pin DIP or 16-pin SOIC package is particularly attractive where overall size is important.

Since the AD1866 provides dc bias voltages, the entire signal chain can be dc coupled. This eliminates ac coupling capacitors from the signal path, improving low frequency performance and lowering system cost and size.

In summary, the AD1866 is an excellent choice for multimedia, battery operated portable or automotive digital audio systems. In the following sections, some examples of high performance audio applications featuring the AD1866 are described.

AD1866 with the Sony CXD2550P Digital Filter

Figure 11 illustrates a 16-bit CD player design incorporating an AD1866 DAC, a Sony CXD2550P digital filter, and 2-pole antialias filters. This high performance, single supply design operates at 8× F_S and is suitable for portable and automotive applications. In this design, the CXD2550P filter transmits left and right channel digital data to the AD1866. The left and right latch signals, LL and LR, are both provided by the word clock signal (LRCKO) of the digital filter. The digital data is converted to low distortion output voltages by the output amplifiers on the AD1866. Also, no deglitching circuitry or external adjustments are required. Bypass capacitors, noise reduction capacitors and the antialias filter details are omitted for clarity.

ADDITIONAL APPLICATIONS

In addition to CD player designs, the AD1866 is suited for similar applications such as DAT, portable musical instruments, laptop and notebook personal computers, and PC audio I/O boards. The circuit techniques illustrated here are directly applicable in those applications. Figures 12, 13, 14, and 15 show connection diagrams for the AD1866 and several popular digital filter chips from NPC and Yamaha. Each application operates at 8× F_S operation. Please refer to the appropriate sections of this data sheet for additional information.

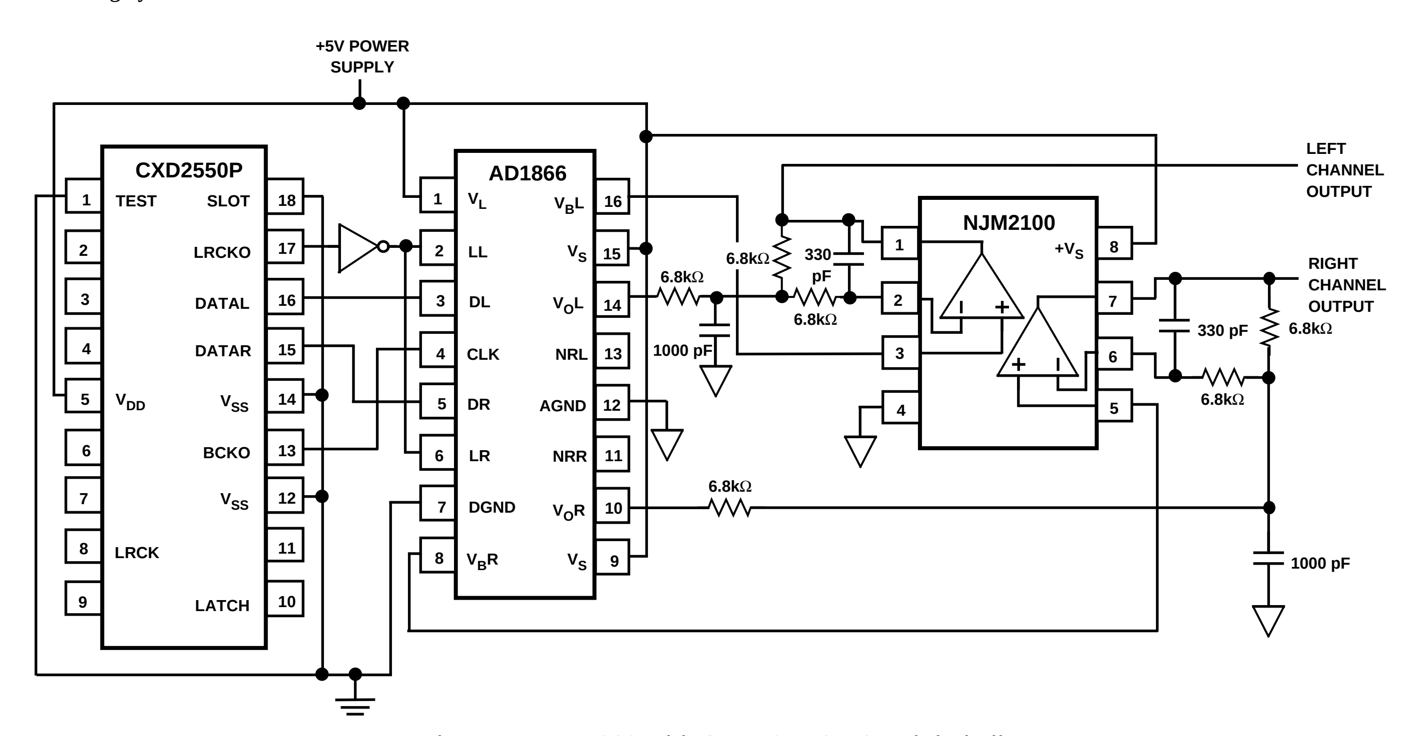


Figure 11. AD1866 with Sony CXD2550P Digital Filter

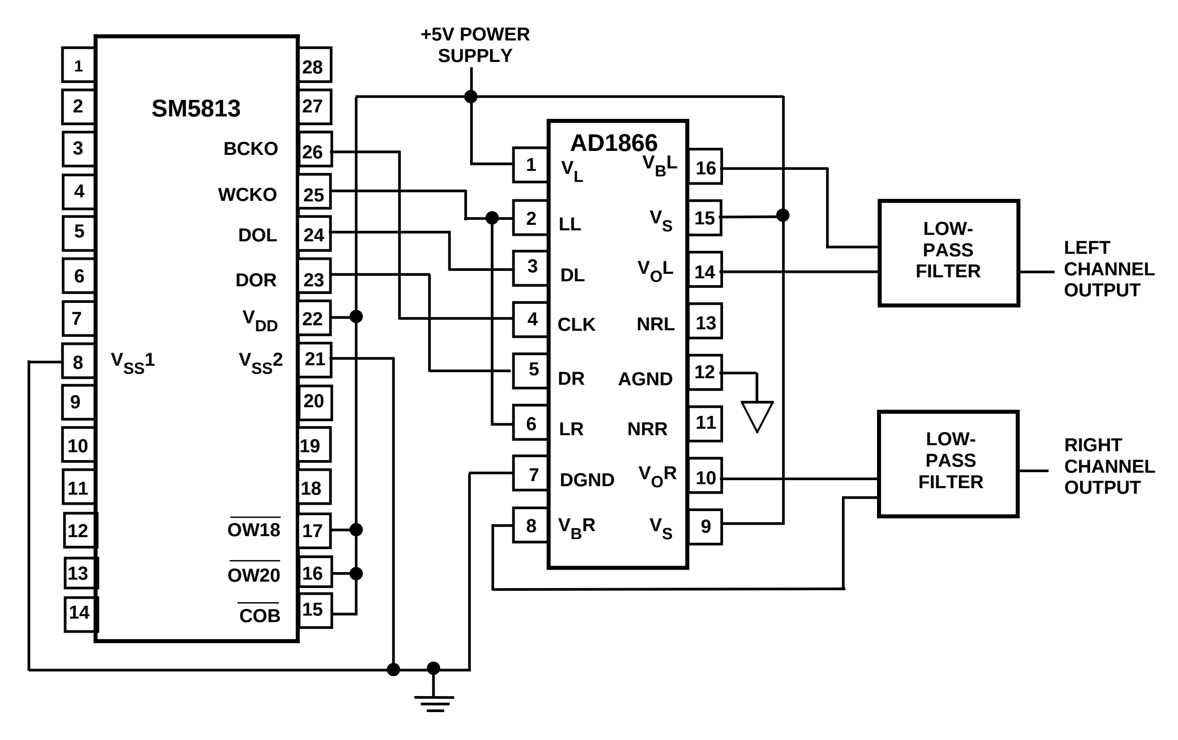


Figure 12. AD1866 with NPC SM5813 Digital Filter

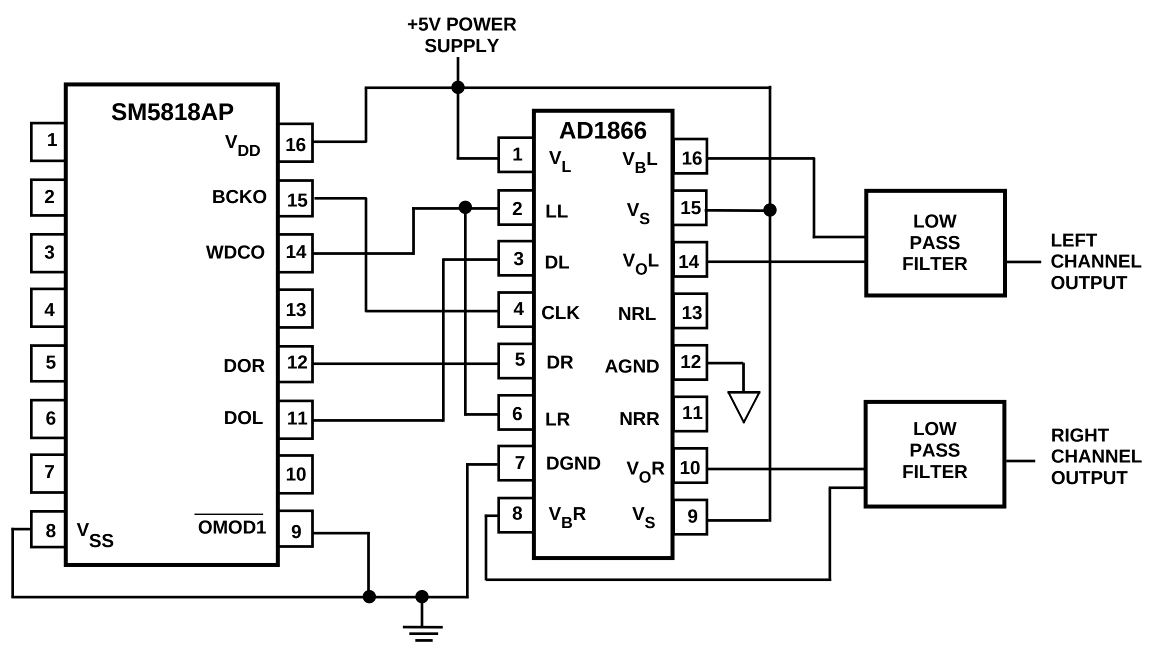


Figure 13. AD1866 with NPC SM5818AP Digital Filter

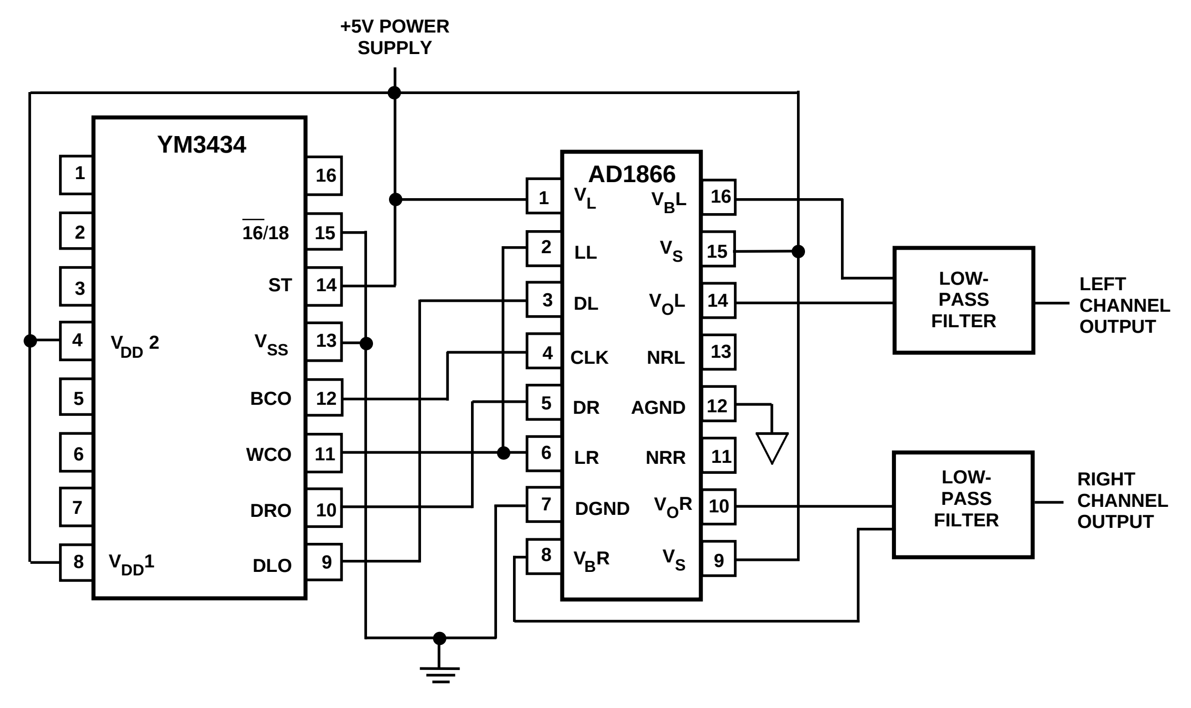


Figure 14. AD1866 with Yamaha YM3434 Digital Filter

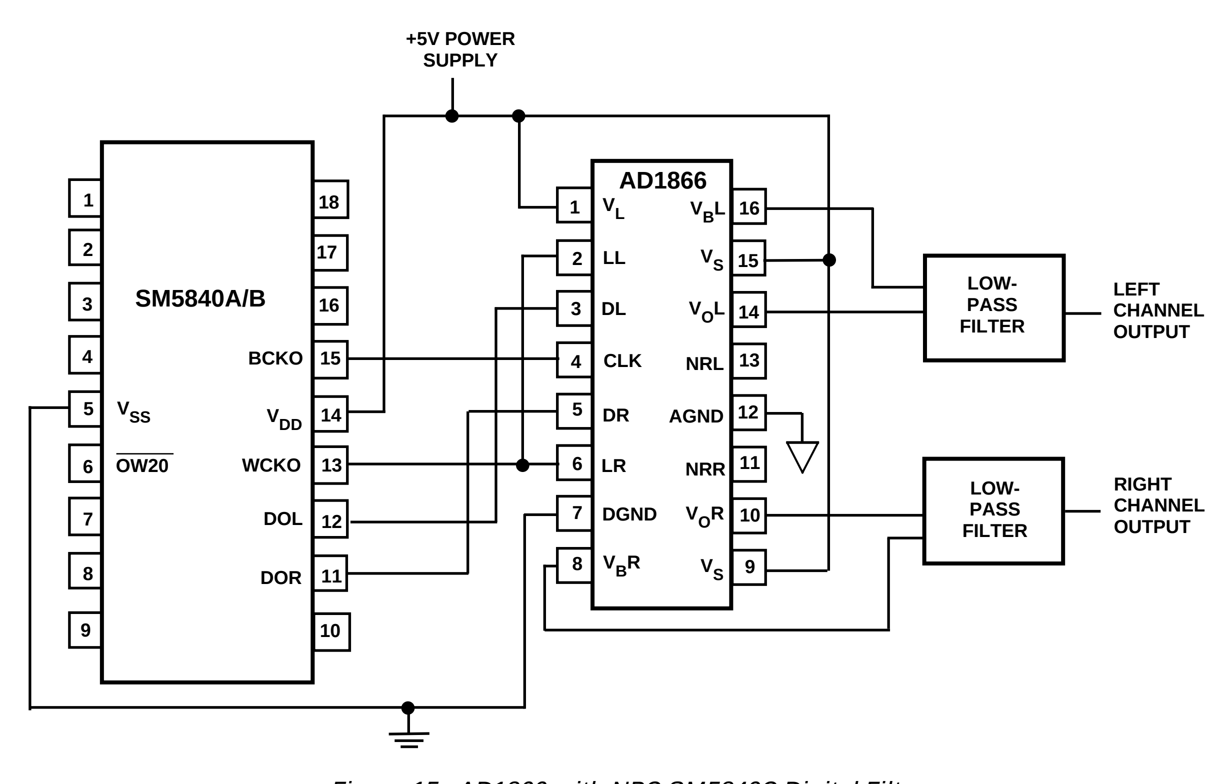
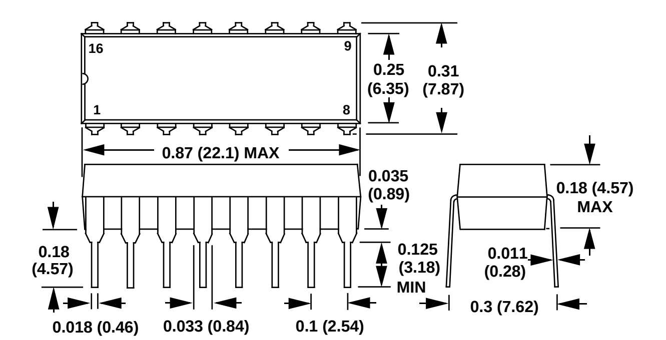


Figure 15. AD1866 with NPC SM5840C Digital Filter

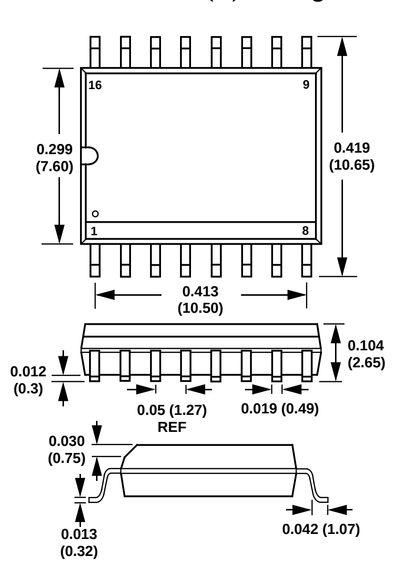
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Plastic DIP (N) Package



Plastic SOIC (R) Package



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